REMARKS

Claims 1-25 are pending. Claims 1, 12, 17, and 24 are independent claims. Reconsideration and allowance of the above-referenced application are respectfully requested.

Claims 1-4, 7-9, 17-19, 24, and 25 stand rejected under 35 U.S.C. 102(b) as allegedly being anticipated by Cheriton et al. (US 6,091,725), hereinafter "Cheriton." Claims 5, 6, 12-16, and 20 stand rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over Cheriton. Claims 10, 11, and 21-23 stand rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over Cheriton in view of applicant's admitted prior art, hereinafter "AAPA." The rejections are respectfully traversed.

Claim 1 recites, "receiving a routing address comprising at least two routing identifiers; and building a routing matrix to use in determining route identification operations to be performed, the routing matrix identifying one or more of the at least two routing identifiers that are to be used in routing." (Emphasis added). Cheriton does not disclose all the features recited in claim 1. In this regard, Cheriton does not describe or suggest building a routing matrix, as recited in claim 1.

Cheriton describes a technique for processing network datagram packets in network devices based on the source-destination address pair contained in the datagram packet itself (col. 4, lines 58-61). Datagram packets received on an input port are buffered in the shared memory buffer. The source-destination address pair in the datagram packet header is used to index the virtual path cache to find a matching entry. If a matching entry is found in the virtual path cache, then the switch hardware performs all the packet processing steps indicated in the virtual path record, including traffic management and packet routing. If no matching entry is found in

the virtual path cache, then the datagram packet is forwarded to the controller CPU for general purpose processing. The controller CPU determines how to process further datagram packets with this source-destination address in the switch hardware. The controller CPU then loads an appropriate entry into the virtual path cache. See col. 5, lines 30-46.

The Office Action states (Office Action, page 3, first paragraph):

> While Cheriton may not specifically disclose the words "building" or "built" in the described invention, the "virtual path cache 415" of Cheriton is inherently "built" as broadly recited in applicant's claims. (Emphasis added).

It is respectfully submitted that reliance on inherence, as described in the Office Action, is inappropriate. In this regard, MPEP, Section 2131 states:

> "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v/ Union Oil Co. of California*, 814, F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).

Further, MPEP, Section 2112, IV states:

> *In re Oelrich*, 666 F.2d 578, 581-82, 212 USPQ 323, 326 (CCPA 1981). "To establish inherency, the extrinsic evidence 'must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill. Inherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient.'" (Emphasis added).

The Office Action states, in part, "the 'virtual path cache 415' of Cheriton is inherently 'built'." The Office Action does not establish that the virtual path cache index is necessarily built in Cheriton. The cited portion of Cheriton (Cheriton,

col. 11, lines 41-42) states, "checking said table of routing information for an entry matching said index value." Thus the cited portion of Cheriton describes checking the table of routing information. The cited portion does not describe building a routing matrix, as recited in claim 1.

Further, Cheriton states (Cheriton, col. 5, lines 25-29):

> The network switch hardware provides a multiplicity of network ports, a shared memory buffer for storing diagram packets, a virtual path cache that stores the state and processing instructions specific to the active datagram packet flows. (Emphasis added).

Thus, as described in Cheriton, a virtual path cache is provided by the network switch hardware. The virtual path cache is not built, as stated in the Office Action. Therefore, Cheriton does not describe building a routing matrix, as recited in claim 1.

Furthermore, claim 1 in Cheriton recites, in part, "A method for operating a packet switching network wherein forwarding is done in a hop-by-hop manner, said network including a plurality of stations, each station having a table of routing information, one or more output ports and one or more input ports…" (Emphasis added). Thus, as recited in Cheriton, each station has a table of routing information. Therefore, neither the cited portion nor any other portion of Cheriton describes or suggests building a routing matrix, as recited in claim 1. Therefore, inherency is not established.

Accordingly, claim 1 should be patentable. Claims 2-11 should also be patentable at least for the same reasons and the additional recitations that they contain.

For example, claim 5 recites, "wherein comparing the destination address comprises using blocks smaller than a length of a shortest of the two or more routing identifiers."

(Emphasis added). The Office Action contends that it would have been obvious to modify the teachings of Cheriton to adjust, vary, select, or optimize the numerical parameters or values of any system. In this regard, the Office Action states, "However, it is generally considered to be within the ordinary skill in the art to adjust, vary, select, or optimize the numerical parameters or values of any system absent a showing of criticality in a particular recited value." (Emphasis added). See, Office Action, page 8, No.6. It is respectfully submitted that the claimed subject matter is unrelated to a particular recited value.

No portion of claim 5 recites a numerical value. The subject matter of claim 5 covers a relationship between a processing activity, namely "comparing," and data being processed, namely "blocks smaller than a length of a shortest of the two or more routing identifiers." Thus, no portion of claim 5 recites a numerical value. Since no portion of claim 5 recites a value, varying, selecting, or optimizing a numerical parameter or value is inapplicable to the subject matter of claim 5. Therefore, reliance on *In re Mason*, *Marconi Wireless Telegraph Co. v U.S.*, *In re Schneider*, *In re Aller*, *In re Saether*, *In re Antonie*, *In re Boesch*, and any other case law related to adjusting, varying, selecting, or optimizing numerical parameters or values is inappropriate. Also, as discussed previously, Cheriton does not describe building a routing matrix. Therefore, Cheriton does not describe all the features of claim 5. Claim 5 should be allowable also for this reason.

Further, for example, claim 10 recites, "wherein route identification operations include a direct lookup operation, a longest-prefix-match lookup operation, and a hash table lookup operation." The Office Action contends that it would have been

obvious to implement the teachings of Cheriton and include a longest-prefix-match lookup operation. This contention is respectfully traversed.

MPEP, Section 2143.01, III states:

> The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. *In re Mills*, 916 F.2d 680, 16 USPQ2d 1430 (Fed. Cir. 1990)…"

Thus, the mere fact that route identification operations such as a direct lookup operation, a longest-prefix-match lookup operation, and a hash table lookup operation were known is not evidence of obviousness to combine Cheriton with the longest-prefix-match lookup operation, as suggested by the Office Action. Further, as discussed previously, Cheriton does not describe building a routing matrix. Therefore, Cheriton does not describe all the features of claim 10. Claim 10 should be allowable also for this reason.

Claim 12 recites, "receiving a source address and a destination address, each comprising at least two routing identifiers; performing an EXCLUSIVE OR operation of the source address routing identifiers with the destination address routing identifiers to produce an address comparison result; and determining a set of route identification operations to perform based upon one or more non-zero values in the address comparison result, wherein a different route identification operation is to be used for each of the one or more non-zero values." (Emphasis added). Cheriton does not disclose all the features recited in claim 12.

The Office Action states, "…Cheriton teaches…determining a set of route identification operations to perform (e.g., determining which virtual path record to output, see col. 9,

lines 34-43)." See, Office Action, page 9, last paragraph. This contention cannot be supported. The cited portion of the Office Action (Cheriton, col. 9, lines 34-43) states:

> The virtual path index 630, which is the source-destination address pair of the incoming datagram, enters hash function 631 which in turn produces a virtual path cache index 632 which in turn looks up the four parallel sets of the virtual path cache SRAMs 601 through 604. The tag field 310 from each set of SRAMs will be compared against the virtual path index 630 and only that virtual path record that matches will be output on the virtual path record databus 633 via tri-state drivers 621 through 624. Combinatorial logic 634 will generate a high signal 635 to indicate a hit. (Emphasis added).

Further, Cheriton (col. 9, lines 44-46) states:

> If no tag field matches, then combinatorial logic 634 will generate a low signal 635 to indicate a miss, i.e., that no valid virtual path record was found in the virtual path cache. (Emphasis added).

Thus, as described in Cheriton, the source-address destination pair is compared to the virtual path index and, based on the comparison, either a high signal is generated to indicate a hit or a low signal is generated to indicate a miss. Neither the cited portion nor any other portion of Cheriton describes or suggests determining a set of route identification operations to perform based upon one or more non-zero values in the address comparison result, as recited in claim 12.

Further, the Office Action fails to acknowledge or address the statements presented in this regard in the Reply to Office Action dated August 14, 2006. Instead the Office Action contends that it would have been obvious to implement the system of Cheriton with index values comprising at least one non-zero value. See, e.g., Office Action, page 3, paragraph 2.

The claim recites, in part, "determining a set of route identification operations to perform based upon one or more non-

zero values in the address comparison result." The claimed subject matter is unrelated to the suggested combination of the system of Cheriton with index values comprising at least one non-zero value. The Office Action fails to acknowledge or address the fact that neither the cited portion nor any other portion of Cheriton describes or suggests determining a set of route identification operations to perform based upon one or more non-zero values in the address comparison result, as recited in claim 12. Instead, the Office Action contends that it would have been obvious to implement the system of Cheriton with index values comprising at least one non-zero value.

Therefore, it is respectfully submitted that regardless of whether or not it would have been obvious to implement the system of Cheriton with index values comprising at least one non-zero value, Cheriton does not describe determining a set of route identification operations to perform based upon one or more non-zero values in the address comparison result, as recited in claim 12. Thus, Cheriton does not describe all the features recited in claim 12. Therefore, a prima facie case of obviousness is not established.

Accordingly, claim 12 should be patentable. Claims 13-16 should also be patentable at least for this reason and the additional recitations that they contain.

Claim 17 recites, "a processor; a network device; a first bus coupled with the network device and with the processor; a memory system embodying information indicative of instructions to cause the processor to perform operations comprising receiving a source address and a destination address, each comprising at least two routing identifiers, and determining a set of route identification operations to perform based upon one or more differences between the source address routing identifiers and the destination address routing identifiers; and

a second bus coupled with the memory system and with the processor." (Emphasis added).

Cheriton does not disclose all the features recited in claim 17. In this regard, Cheriton does not describe or suggest determining a set of route identification operations to perform based upon one or more differences between the source address routing identifiers and the destination address routing identifiers, as recited in claim 17. The Office Action states, "...Cheriton teaches determining a set of route identification operations to perform (e.g., determining which virtual path record to output, see col. 9, lines 34-43)." As discussed previously, the cited portion of Cheriton describes comparing the source-address destination pair to the virtual path index and, based on the comparison, generating either a high signal to indicate a hit or a low signal to indicate a miss. Thus, neither the cited portion nor any other portion of Cheriton describes or suggests determining a set of route identification operations to perform based upon one or more differences between the source address routing identifiers and the destination address routing identifiers, as recited in claim 17. Further, no portion of Cheriton describes or suggests that the source address or destination address includes at least two routing identifiers. In contrast, claim 17 recites, in part, "receiving a source address and a destination address, each comprising at least two routing identifiers." (Emphasis added). Therefore, Cheriton does not describe all the features recited in claim 17.

Accordingly, claim 17 should be patentable. Claims 18-23 should also be patentable at least for the same reasons and the additional recitations that they contain.

Claim 24 recites, "means for receiving a source address and a destination address, each comprising at least two routing identifiers; means for using the processor to identify one or

more differences between the source address routing identifiers and the destination address routing identifiers; means for determining a set of route identification operations based upon the one or more differences, wherein a different route identification operation is determined for each of the one or more differences; and means for routing data based upon the set of route identification operations." (Emphasis added).

Thus, claim 24 should be patentable at least for reasons similar to claim 17. Claim 25 should also be patentable at least for the same reasons and the additional recitations that it contains.

CONCLUSION

In view of the amendments and remarks herein, claims 1-25 are in condition for allowance and a notice of allowance is respectfully requested. It is believed that all of the pending claims have been addressed. However, the absence of a reply to a specific issue or comment does not signify agreement with or concession of that issue or comment. Because the arguments made above may not be exhaustive, there may be reasons for patentability of any or all pending claims (or other claims) that have not been expressed. Finally, nothing in this paper should be construed as an intent to concede any issue with regard to any claim, except as specifically stated in this paper, and the amendment of any claim does not necessarily signify concession of unpatentability of the claim prior to its amendment.

It is respectfully suggested for all of these reasons, that the current rejections are overcome, that none of the cited art teaches or suggests the features which are claimed, and therefore that all of these claims should be in condition for allowance. A formal notice of allowance is thus respectfully requested.

Please apply any charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

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